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I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 2002-268315 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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[NAME OF DOCUMENT] SPECIFICATION  
[TITLE OF INVENTION] NONVOLATILE SEMICONDUCTOR  
MEMORY DEVICE  
[SCOPE OF CLAIMS]

- 5 [CLAIM 1] A nonvolatile semiconductor memory device,  
comprising:  
a plurality of blocks each having a  
nonvolatile memory cell array; and  
a program potential generating circuit  
10 which supplies a program potential to the  
nonvolatile memory cell array,  
wherein said program potential generating  
circuit adjusts the program potential according to a  
first address signal selecting one of said blocks  
15 and a second address signal indicating a position of  
a write-accessed memory cell in said one of said  
blocks.  
[CLAIM 2] The nonvolatile semiconductor memory  
device as claimed in claim 1, wherein said program  
20 potential generating circuit includes:  
a booster circuit which generates a  
boosted potential; and  
a regulator circuit which generates the  
program potential according to the boosted potential  
25 and a reference potential, wherein the program  
potential generated by said regulator circuit is  
adjusted according to the first address signal and  
the second address signal.  
[CLAIM 3] The nonvolatile semiconductor memory  
30 device as claimed in claim 2, wherein said regulator  
circuit includes:  
a capacitance circuit which generates a  
comparison potential by dividing the program  
potential by use of capacitances;  
35 a differential amplifier circuit which  
generates the program potential from the boosted  
potential in response to a comparison between the

comparison potential and the reference potential;  
and

a circuit which adjusts the capacitances  
of said capacitance circuit according to the first  
5 address signal and the second address signal.

[CLAIM 4] The nonvolatile semiconductor memory  
device as claimed in claim 1, further comprising a  
program potential adjusting circuit which generates  
a program potential adjusting signal according to  
10 the first address signal and the second address  
signal, wherein said program potential generating  
circuit adjusts the program potential according to  
the program potential adjusting signal.

[CLAIM 5] The nonvolatile semiconductor memory  
15 device as claimed in claim 4, wherein said program  
potential adjusting circuit performs inversion  
control that either inverts or does not invert the  
second address signal, depending on the first  
address signal, and supplies the second address  
20 signal having undergone the inversion control to  
said program potential generating circuit as the  
program potential adjusting signal.

[CLAIM 6] The nonvolatile semiconductor memory  
device as claimed in claim 1, wherein two of said  
25 blocks have different arrangements of a second  
address represented by the second address signal  
such that the second address is arranged in reversed  
orders between the two blocks in relation to  
distance from said program potential generating  
30 circuit, the program potential being adjusted  
according to the second address signal after  
identifying one of the two blocks according to the  
first address signal, such as to reflect a physical  
distance from said program potential generating  
35 circuit to the position of the write-accessed memory  
cell.

[CLAIM 7] The nonvolatile semiconductor memory

device as claimed in claim 1, wherein two of said blocks are positioned at different distances from said program potential generating circuit, the program potential being adjusted according to the  
5 second address signal after identifying one of the two blocks according to the first address signal, such as to reflect a physical distance from said program potential generating circuit to the position of the write-accessed memory cell.

10 [DETAILED DESCRIPTION OF INVENTION]

[Field of Invention]

The present invention generally relates to nonvolatile semiconductor memory devices, and particularly relates to a nonvolatile semiconductor  
15 memory device in which a memory cell array is divided into a plurality of blocks.

[Description of Conventional Art]

When data is to be written into a flash memory, high potential is applied to the gate and  
20 drain of a memory cell, thereby injecting channel hot electron into the floating gate. The potential applied to the drain of the memory cell is preferably set to as high potential as possible when considering the speed of data writing. If this  
25 potential is too high, however, drain disturb occurs at memory cells that are not selected. This causes charge loss, i.e., electron trapped in the floating gate leaks. The potential applied to the drain should thus be set within a predetermined range.

30 In conventional flash memories, such drain potential is set to a predetermined level by a booster circuit and a regulator circuit. As the length of bit lines increases together with the size of flash memories, a potential drop caused by bit-  
35 line resistance becomes increasingly noticeable when electric currents run through bit lines. This is especially so near the endpoint of the bit lines.

This makes it difficult to set the drain potential at the time of write operations within a predetermined range with respect to all the memory cells.

5                   In order to obviate this problem, Japanese  
Patent Application No. 2001-303709, which was filed  
by the same applicant as this application, adjusts a  
potential regulated by a regulator circuit according  
to address signals that determine the position of  
10   accessed memory cells, thereby setting the drain  
potential within a predetermined range. The  
regulator circuit divides a boosted potential  
generated by a booster circuit by use of a series  
connection of condensers, and adjusts the output  
15   potential (drain potential) according to the  
comparison of the divided potential with a reference  
potential. The capacitances of the condensers are  
controlled based on the address signals, thereby  
adjusting the output potential in accordance with  
20   the position (i.e., address position) on the bit  
lines.

A further example of the related art  
(Patent Document 1) adjusts a potential by which  
data is written.

25           [Patent Document 1]  
              Japanese Patent Application Publication No.  
11-297086

[Problems to be Solved by Invention]

              In semiconductor memory devices such as  
30   flash memories, provision is often made to provide a  
memory cell array that is divided into a plurality  
of blocks. Such division into blocks can reduce the  
load on bit lines and word lines, providing the  
advantage of high-speed data access. In the multi-  
35   block configuration, only one set of a booster  
circuit and a regulator circuit is generally  
provided, and the output of the regulator circuit is

supplied to each memory cell in each block. In such a case, the distance from the regulator circuit to memory cells is not related to addresses in a straightforward manner. Because of this, the  
5 technology disclosed in the above-cited patent application does not properly work where a memory cell array is divided into blocks.

Accordingly, the present invention is aimed at supplying a constant data-write potential  
10 to memory cells regardless of the position of the memory cells even when a memory cell array is divided into a plurality of blocks.

[Means to Solve Problems]

A nonvolatile semiconductor memory device  
15 according to the present invention includes a plurality of blocks each having a nonvolatile memory cell array, and a program potential generating circuit which supplies a program potential to the nonvolatile memory cell array, wherein the program  
20 potential generating circuit adjusts the program potential according to a first address signal selecting one of the blocks and a second address signal indicating a position of a write-accessed memory cell in the noted one of the blocks.

25 The nonvolatile semiconductor memory device described above adjusts the program potential according to the first address signal identifying a block and the second address signal specifying the position of a write-accessed memory cell in the  
30 identified block. Accordingly, the distance from the program potential generating circuit to each memory block and the addressing configuration of each memory block are taken into account for the purpose of adjusting the program potential. This  
35 provides for a proper program potential to be generated with respect to each memory cell location within each memory block.



[Embodiments for Carrying out the Invention]

In the following, embodiments of the present invention will be described with reference to the accompanying drawings.

5           Fig.1 is a block diagram of a nonvolatile semiconductor memory device according to the present invention.

          A nonvolatile semiconductor memory device  
10 of Fig.1 includes a state-control circuit 11, an input/output buffer 12, an address latch 13, an X decoder 14, a Y decoder 15, a cell array 16, a Y gate 17, a data latch 18, a program-potential generating circuit 19, an erasure-potential generating circuit 20, a chip-enable/output-enable  
15 circuit 21, a sector erasure circuit 22, and a program-potential adjusting circuit 23.

          The state-control circuit 11 receives a write-enable signal WE, a chip-enable signal CE, data signals DQ0 through DQ15, etc., as control  
20 signals from the exterior of the device, and operates as a state machine based on the control signals, thereby controlling the operation of each part of the nonvolatile semiconductor memory device 10.

25           The input/output buffer 12 receives data DQ0 through DQ15 from the exterior of the device, and supplies the received data to the state-control circuit 11 and the data latch 18. The address latch 13 latches address signals ADD supplied from the  
30 exterior of the device, and supplies these address signals to the X decoder 14 and the Y decoder 15. The X decoder 14 decodes the address supplied from the address latch 13, and activates a word line provided in the cell array 16 in response to the  
35 decoding results. The Y decoder 15 decodes the address supplied from the address latch 13, and controls the Y gate 17 in response to the decoding

results, thereby selectively retrieving data from the bit lines of the cell array 16 for transfer to the data latch 18.

The cell array 16 includes an array of  
5 memory cell transistors, word lines, bit lines, etc.,  
and stores data in each memory cell transistor. At  
the time of data reading, data are read from memory  
cells selected by the activated word line, and are  
supplied to the bit lines. At the time of  
10 programming and erasing, word lines and bit lines  
are set to potentials suitable for respective  
operations, thereby injecting or removing electric  
charge into or from memory cells. Although not  
explicitly shown in Fig.1, the cell array 16 is  
15 comprised of a plurality of blocks, and peripheral  
circuitry such as the X decoder 14 and the Y decoder  
15 is also provided on a block-by-block basis.

The data latch 18 compares a reference  
current of a reference cell with a data current that  
20 is supplied from the cell array 16 according to  
selection by the Y decoder 15 and the X decoder 14.  
This provides the sensing of data as to whether it  
is 0 or 1. The sensed data is supplied as read data  
to the input/output buffer 12. Further, a verify  
25 check for a program operation or an erase operation  
is performed by comparing a reference current of a  
program-verify reference cell or an erase-verify  
reference cell with a data current, which is  
supplied from the cell array 16 according to  
30 selection by the Y decoder 15 and the X decoder 14.

The program-potential generating circuit  
19 operates under the control of the state-control  
circuit 11 to generate a program potential (i.e., a  
boosted potential for use in programming). The  
35 program potential is used to drive the X decoder 14  
and the Y decoder 15, thereby performing data-write  
operations with respect to the cell array 16,

according to write data that is supplied from the input/output buffer 12 to the data latch 18. The erasure-potential generating circuit 20 generates an erasure potential that is to be supplied to word lines and bit lines at the time of an erase operation. The erasure potential is supplied to the sector erasure circuit 22. The sector erasure circuit 22 carries out an erase operation on a sector-specific basis.

10           The chip-enable/output-enable circuit 21 receives a chip-enable signal CE and an output-enable signal OE as control signals from the exterior of the device, and determines whether to drive the input/output buffer 12 and the cell array 15 16.

          The program-potential adjusting circuit 23 is a circuit characteristic to the present invention, and generates a program-potential adjusting signal VPROG\_ADJ based on the address signals ADD for transmission to the program-potential generating circuit 19. The program-potential generating circuit 19 adjusts the program potential according to the program-potential adjusting signal VPROG\_ADJ.

25           Fig.2 is a drawing showing an embodiment of the program-potential adjusting circuit 23 and the program-potential generating circuit 19 according to the present invention.

          In an example of Fig.2, the cell array 16 is divided into two blocks, i.e., a cell array 16A and a cell array 16B. The cell array 16A includes memory cell sets 16A-0 through 16A-3 and a sector-redundancy memory cell set 16A-R. The cell array 16B includes memory cell sets 16B-0 through 16B-3 and a sector-redundancy memory cell set 16B-R.

35           Bit lines of the cell arrays 16A and 16B are coupled to a regulator 31 via gates 38 and 39, respectively. The gates 38 and 39 are controlled by

use of the most significant bit A23 of address signals. The gate 38 opens when the bit A23 is HIGH, and the gate 39 is opened by an inverter 37 when the bit A23 is LOW.

5           The regulator 31 is part of the program-potential generating circuit 19. The regulator 31 operates in such a manner as to adjust a boosted potential DPUMP to a predetermined potential as the boosted potential DPUMP is generated by a booster  
10 circuit (i.e., boosted-potential generating circuit) 19A of the program-potential generating circuit 19. Such potential adjustment by the regulator 31 is controlled by the program-potential adjusting signal VPROG\_ADJ(1:0) comprised of two bits.

15           In the example of Fig.2, the program-potential adjusting circuit 23 includes program-potential adjusting units 32 and 33, gates 35 and 36, and an inverter 34. Each of the program-potential adjusting units 32 and 33 generates the two-bit  
20 program-potential adjusting signal VPROG\_ADJ(1:0). The most significant bit A23 of address signals selects one of the program-potential adjusting signals VPROG\_ADJ(1:0). The selected program-potential adjusting signal VPROG\_ADJ(1:0) is  
25 supplied to the regulator 31.

Fig.3 is a circuit diagram showing an example of the regulator 31.

30           The regulator 31 of Fig.3 includes a differential amplifier 41, a transistor 42, a condenser 43, transistors 44 through 47, condensers (MOS capacitances) 48 through 51, inverters 52 through 55, NAND circuits 56 through 59, and an inverter 60. The differential amplifier 41 is powered by the boosted potential DPUMP generated by  
35 the booster circuit 19A, and generates a program potential VPROG in response to a difference between the potential at a node N1 and a reference potential

VREFD. In detail, the program potential VPROG is raised when the potential at the node N1 is lower than the reference potential VREFD, whereas the program potential VPROG is lowered when the potential at the node N1 is higher than the reference potential VREFD. The potential at the node N1 is equal to a fraction of the program potential VPROG divided by the condenser 43. Control as described above thus adjusts the program potential VPROG to a predetermined potential.

The potential at the node N1 is determined by a ratio of the capacitance of the condenser 43 to the capacitance of a selected one of the condensers 48 through 51. Accordingly, it is possible to control the level of the program potential VPROG by selecting one of the condensers 48 through 51.

In this example, the condensers 48 and 49 or the condensers 50 and 51 are chosen according to the most significant bit A23 of the address signals. If the address bit A23 is HIGH, for example, the condensers 48 and 49 are selected. As was described with reference to Fig.2, the cell array 16A is coupled to the regulator 31 when the address bit 23 is HIGH. In this case, therefore, the condensers 48 and 49 are coupled to the cell array 16A.

The two-bit program-potential adjusting signal VPROG\_ADJ(1:0) controls the conductive/non-conductive state of the transistors 44 and 45 so as to control the selected/unselected state of each of the condensers 48 and 49. The program-potential adjusting signal VPROG\_ADJ(1:0) corresponds to two bit address signals for selecting the memory cell sets 16A-0 through 16A-3. The program-potential adjusting signal VPROG\_ADJ(1:0) is (0,0) when the memory cell set 16A-0 is selected for writing, (0,1) when the memory cell set 16A-1 is selected for writing, (1,0) when the memory cell set 16A-2 is

selected for writing, and (1,1) when the memory cell set 16A-3 is selected for writing. In addition, the program-potential adjusting signal VPROG\_ADJ(1:0) is also set to (1,1) when the sector-redundancy memory cell set 16A-R is selected. In this manner, capacitance that is coupled in series to the capacitance of the condenser 43 is changed to control the potential at the node N1, thereby adjusting the program potential VPROG.

10 In Fig.2, the memory cell arrays 16A and 16B are positioned at respective distances from the regulator 31 as represented by distance L1 and distance L2, respectively. The regulator 31 thus needs to provide different program potentials to reflect the difference in the distance. To this end, the condensers 48 and 49 are selected for the cell array 16A when the address bit A23 is HIGH, while the condensers 50 and 51 are selected for the cell array 16B when the address bit A23 is LOW.

20 In the example of Fig.2, the program-potential adjusting units 32 and 33 are provided for the cell arrays 16A and 16B, respectively. This is to ensure that different address configurations between the cell arrays 16A and 16B can be properly taken care of. For example, there may be a case in which an address (0,0) is assigned to the memory cell set 16A-0 at the closest position in the cell array 16A whereas an address (0,0) is assigned to the memory cell set 16B-3 at the farthest away position in the cell array 16B. Even in such a case, the program-potential adjusting unit 33 corresponding to the cell array 16B may manipulate the logic of relevant address bits to generate the program-potential adjusting signal VPROG\_ADJ(1:0) conforming to the address configuration of the cell array 16B.

Fig.4 is a block diagram showing the

construction of four blocks into which a memory cell array is divided.

In Fig.4, the memory cell array is divided into four blocks, i.e., cell arrays 16A through 16D. At the center of the four blocks is located the program-potential generating circuit 19. The program potential VPROG generated by the program-potential generating circuit 19 is supplied to X gates 17A through 17D of the respective blocks. As shown in Fig.4, the memory cell sets 16A-0 through 16A-3 of the cell array 16A are selected when the two corresponding bits A21 and A20 of the address signals are (0,0), (0,1), (1,0), and (1,1), respectively. The memory cell sets 16B-0 through 16B-3 of the cell array 16B are selected when the two corresponding bits A21 and A20 of the address signals are (1,1), (1,0), (0,1), and (0,0), respectively. Since the cell array 16A and the cell array 16B have different address configurations, the program-potential adjusting circuit 23 needs to supply different program-potential adjusting signals VPROG\_ADJ(1:0) in respect of the respective cell arrays.

Fig.5 is a circuit diagram showing an example of the program-potential adjusting circuit 23 used in the construction of Fig.4. As shown in Fig.2, the program-potential adjusting circuit 23 may generate the program-potential adjusting signals VPROG\_ADJ(1:0) separately for the cell arrays 16A and 16B by use of the program-potential adjusting units 32 and 33. Unlike this, the construction shown in Fig.5 achieves all the necessary logic operations, inclusive of the operation of redundancy selection, by use of a single circuit.

The program-potential adjusting circuit 23 of Fig.5 includes a NAND gate 71, inverters 72 through 78, PMOS transistors 79 through 90, and NMOS

transistors 91 through 103. The program-potential adjusting circuit 23 receives two bits A20 and A21 of the address signals, and outputs the two-bit program-potential adjusting signal VPROG\_ADJ(1:0).

- 5 The output of the inverter 77 is a program-potential adjusting signal VPROG\_ADJ(1) that corresponds to the address bit A21, and the output of the inverter 78 is a program-potential adjusting signal VPROG\_ADJ(0) that corresponds to the address bit A20.
- 10 The program-potential adjusting signal VPROG\_ADJ(1) and the program-potential adjusting signal VPROG\_ADJ(0) are put together to be represented as the two-bit signal VPROG\_ADJ(1:0).

- Fig.6 is a logic-value table that shows
- 15 inputs and outputs of the logic circuit shown in Fig.5.

- As shown in Fig.5 and Fig.6, a program instruction signal PGM, a redundancy instruction signal HIT, and the most significant address bit A23
- 20 are input in addition to the address signals A20 and A21. The program instruction signal PGM becomes HIGH when a programming operation is performed. The redundancy instruction signal HIT becomes HIGH when a redundancy operation is carried out. The circuit
- 25 outputs are the two-bit program-potential adjusting signal VPROG\_ADJ(1:0).

- As shown in Fig.6, the program-potential adjusting signal VPROG\_ADJ(1:0) is (L, L) if the program instruction signal PGM is LOW indicative of
- 30 no program operation, regardless of the signal levels of other signals. When a program operation is performed, i.e., when the program instruction signal PGM is HIGH, the circuit output varies depending on the signal levels of the redundancy
- 35 instruction signal HIT and the address signal A23. If the redundancy instruction signal HIT is HIGH, the program-potential adjusting signal



VPROG\_ADJ(1:0) is (H, H) regardless of the signal level of the address signal A23. This provides for a proper program potential VPROG to be generated by the regulator 31 of Fig.3 and to be supplied to the spare sectors 16A-R and 16B-4, which are located farthest away from the Y gate along the extension of bit lines as shown in Fig.4.

If the redundancy instruction signal HIT is LOW, the program-potential adjusting signal VPROG\_ADJ(1:0) varies depending on the signal level of the address signal A23. As shown in Fig.6, the program-potential adjusting signal VPROG\_ADJ(1:0) is (A21, A20) if the address signal A23 is HIGH. In Fig.4, the memory cell sets 16A-0 through 16A-3 are selected when (A21, A20) is (0,0), (0,1), (1,0), and (1,1), respectively, in the cell array 16A that is chosen in response to the HIGH level of the signal A23. Accordingly, a proper program potential can be supplied to these memory cell sets by having the regulator 31 adjust the program potential according to the program-potential adjusting signal VPROG\_ADJ(1:0) that is no other than (A21, A20).

For example, the memory cell set 16A-0 closest to the Y gate 17A is selected for data writing when (A21, A20) is (0,0). Since the program-potential adjusting signal VPROG\_ADJ(1:0) is (0,0) in this case, the regulator 31 selects the program potential VPROG that corresponds to the closest position. The memory cell set 16A-1 that is second closest to the Y gate 17A is selected for data writing when (A21, A20) is (0,1). Since the program-potential adjusting signal VPROG\_ADJ(1:0) is (0,1) in this case, the regulator 31 selects the program potential VPROG that corresponds to the second closest position.

If the redundancy instruction signal HIT is LOW and the address signal A23 is LOW, the

program-potential adjusting signal VPROG\_ADJ(1:0) becomes (A21B, A20B), as shown in Fig.6, which is an inverse of (A21, A20). In Fig.4, the memory cell sets 16B-0 through 16B-3 are selected when (A21, A20) is (1,1), (1,0), (0,1), and (0,0), respectively, in the cell array 16B that is chosen in response to the LOW level of the signal A23. Accordingly, a proper program potential can be supplied to these memory cell sets by adjusting the program potential according to the program-potential adjusting signal VPROG\_ADJ(1:0) that is an inverse of (A21, A20).

For example, the memory cell set 16B-0 closest to the Y gate 17B is selected for data writing when (A21, A20) is (1,1). Since the program-potential adjusting signal VPROG\_ADJ(1:0) is (0,0) in this case, the regulator 31 selects the program potential VPROG that corresponds to the closest position. The memory cell set 16B-1 that is second closest to the Y gate 17B is selected for data writing when (A21, A20) is (1,0). Since the program-potential adjusting signal VPROG\_ADJ(1:0) is (0,1) in this case, the regulator 31 selects the program potential VPROG that corresponds to the second closest position.

The same applies in the case of the cell arrays 16D and 16D. The program potential is generated for the cell array 16C in the same manner as for the cell array 16A, and is generated for the cell array 16D in the same manner as for the cell array 16B. In the configuration shown in Fig.4, there is no need to select either the condensers 48 and 49 or the condensers 50 and 51 in the regulator 31 according to the address signal A23 if the distance from the regulator 31 is the same for both the cell array 16A and the cell array 16B. In such a case, only on set of condensers (e.g., the condensers 48 and 49) may be provided.

In this manner, the present invention takes into account the distance from the regulator to each memory block and the addressing configuration of each memory block in order to  
5 adjust the program potential according to the address signals. This provides for a proper program potential to be generated with respect to each memory cell location within each memory block.

In the embodiments described above, a  
10 description has been given of a case in which the number of blocks is two or four. The number of memory blocks is not limited to these numbers. Further, a description has been given of a case in which four memory cell sets (five if the redundancy  
15 memory cell set is included) are provided within each memory cell block. The number of memory cell sets may be any number other than four, such as five or a higher number. In such a case, the number of bits that constitute the program-potential adjusting  
20 signal VPROG\_ADJ may be determined according to the step size that is desired for potential adjustment. Even if the number of memory cell sets is 16, for example, a total of four wide steps for potential adjustment may be sufficient. If this is the case,  
25 the number of bits of the program-potential adjusting signal VPROG\_ADJ is set to two. Alternatively, a total of 16 narrower steps for potential adjustment may be desired when the number of memory cell sets is 16. If this is the case, the  
30 number of bits of the program-potential adjusting signal VPROG\_ADJ is set to four.

In the embodiments described above, the program-potential adjusting signal VPROG\_ADJ is comprised of  $n$  bits, and the regulator 31 performs  
35 program-potential adjustment through  $2^n$  adjustment steps. Alternatively, provision may be made to select one condenser corresponding to one of the  $n$

bits of the program-potential adjusting signal  
VPROG\_ADJ, thereby achieving the n-step adjustment  
of a program potential.

Although the present invention has been  
5 described with reference to embodiments, the present  
invention is not limited to these embodiments.  
Various variations and modifications may be made  
without departing from the scope of the claimed  
invention.

10 [Advantage of the Invention]

The nonvolatile semiconductor memory  
device according to the present invention adjusts  
the program potential according to the first address  
signal identifying a block and the second address  
15 signal specifying the position of a write-accessed  
memory cell in the identified block. Accordingly,  
the distance from the program potential generating  
circuit to each memory block and the addressing  
configuration of each memory block are taken into  
20 account for the purpose of adjusting the program  
potential. This provides for a proper program  
potential to be generated with respect to each  
memory cell location within each memory block.

[Brief Description of the Drawings]

25 [Figure 1]

Fig.1 is a block diagram of a nonvolatile  
semiconductor memory device according to the present  
invention.

[Figure 2]

30 Fig.2 is a drawing showing an embodiment  
of a program-potential adjusting circuit and a  
program-potential generating circuit according to  
the present invention.

[Figure 3]

35 Fig.3 is a circuit diagram showing an  
example of a regulator.

[Figure 4]

Fig.4 is a block diagram showing the construction of four blocks into which a memory cell array is divided.

[Figure 5]

5            Fig.5 is a circuit diagram showing an example of a program-potential adjusting circuit used in the construction of Fig.4.

[Figure 6]

10           Fig.6 is a logic-value table that shows inputs and outputs of a logic circuit shown in Fig.5.

[Description of Reference Numerals]

- 11 state-control circuit
- 12 input/output buffer
- 13 address latch
- 15 14 X decoder
- 15 15 Y decoder
- 16 cell array
- 17 Y gate
- 18 data latch
- 20 19 program-potential generating circuit
- 20 20 erasure-potential generating circuit
- 21 chip-enable/output-enable circuit
- 22 sector erasure circuit
- 23 program-potential adjusting circuit

[NAME OF DOCUMENT] ABSTRACT

[ABSTRACT]

[PROBLEM] The present invention is aimed at  
supplying a constant data-write potential to memory  
5 cells regardless of the position of the memory cells  
even when a memory cell array is divided into a  
plurality of blocks.

[SOLUTION] A nonvolatile semiconductor memory device  
includes a plurality of blocks each having a  
10 nonvolatile memory cell array, and a program  
potential generating circuit which supplies a  
program potential to the nonvolatile memory cell  
array, wherein the program potential generating  
circuit adjusts the program potential according to a  
15 first address signal selecting one of the blocks and  
a second address signal indicating a position of a  
write-accessed memory cell in the noted one of the  
blocks.

[SELECTED FIGURE]     FIGURE 1

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